ABSTRACT OF THE DISCLOSURE

A data processing device includes a processor core, and a memory interface portion arranged between the processor core and an external memory mapped into a predetermined external memory space. The memory interface portion includes a fetch circuit for receiving an address value for access to the external memory space from the processor core, and fetching the data at the address in the external memory, a translator for translating the nonnative instruction fetched from the external memory into the native instruction, and a select circuit for selectively applying the data read from the external memory space and the instruction prepared by translating the instruction read from the external memory space by the translator to the processor core depending on whether the address value for the access to the external memory space is in a predetermined region or not.